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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,581	09/30/2003	Gerolf F. Hoflehner	42P16805	7964

45209 7590 09/15/2008

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EXAMINER	
ARCOS, CAROLINE H	

ART UNIT	PAPER NUMBER
2195	

MAIL DATE	DELIVERY MODE
09/15/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/676,581	HOFLEHNER ET AL.	
	Examiner	Art Unit	
	CAROLINE ARCOS	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09/30/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are pending for examination.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

3. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

4. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-20 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 4-8, 11-15 and 17-19 of patent (US 7398521) in view of Mulder ("inter: An inexpensive inter-procedural register allocator" Micro processing and microprogramming, Elsevier Science Publishers, Vol. 27, 1998, Pages 95-100). Although the conflicting claims are not identical, they are not patentably distinct from each other

because both systems comprise substantially the same elements. For example, claims 1, 2, 4 and 5 functions performed by the steps of the instant application are the same and obvious as the steps of claim 1 of patent (US 7398521). (generating, during a compilation of a code having a main thread, one or more threads executable in a data processing system, each of the one or more threads including instructions copied from the main thread / creating, automatically during a compilation of code, a plurality of threads executable in a processor of a data processing system, resulting in a thread tree potentially for at least one function in the code, wherein the thread tree represents a thread dependency graph of the plurality of the threads); (selecting a current thread by traversing the thread tree in a bottom-up order that ensures that all child threads of the current thread had been selected before selecting the current thread as a parent thread/ repeating the selecting, determining, and allocating in a bottom-up order until each of the one or more threads as been processed.); (determining resources allocated to one or more child threads spawned from the current thread; and allocating resources for the current thread in consideration of the resources allocated to the current thread's one or more child threads to avoid resource conflicts between the current thread and its one or more child threads/ determining resources allocated to one or more child threads spawned from the current thread; and allocating resources for the current thread in consideration of the resources allocated to the current thread' s one or more child threads to avoid resource conflicts between the current thread and its one or more child threads);(wherein the resources include at least one of hardware registers and memory used by the respective thread at least one of the one or more child threads/ wherein the allocated resources include one or more hardware registers and physical memory associated with the processor used by each of the plurality of threads); (wherein the resources allocated to the one or

more child threads are recorded in a data structure accessible by the current thread/ wherein the resource allocated to the one or more child threads are recorded in a data structure).

6. The instant application doesn't explicitly state the resulting in a thread tree potentially for at least one function in the code, wherein the thread tree represents a thread dependency graph of the plurality of the threads, and that the resource allocated to the one or more child threads are recorded in a data structure is maintained by a compiler at the compilation to enable the compiler to avoid the resource conflicts between current thread and the one or more child threads such that the processor perform less resource management actions during executing the plurality of the threads by the processor.

7. However, Mulder teaches the resulting in a thread tree potentially for at least one function in the code, wherein the thread tree represents a thread dependency graph of the plurality of the threads (Fig. 9; pg. 98, section 6, lines 1-5; pg. 98, section 6.1, lines 1-10) and it is obvious to one of ordinary skill in the art at the time the invention was made to conclude from Mulder teaching of interface files are type of data structure that is maintained by a compiler to allocate resource starting with the child thread and ending with the parent thread that that the data structure is maintained by a compiler since it is at compilation time to enable the compiler to avoid the resource conflicts between current thread and the one or more child threads such that the processor perform less resource management actions during executing the plurality of the threads by the processor which improve system performance, system speed and eliminate system traffic.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The claim language in the following claims is not clearly understood:

i. As per claim 1, line 3, It is not clearly understood what is meant by "a most bottom order" (i.e. the end of the same chain or tree level "horizontal" or bottom level of the chain or tree "bottom level vertically" ?). It is not clear bottom of what order? (i.e. thread tree order/ thread chain).

ii. i As per claim 8, it has the same deficiency as claim 1.

iii. As per claim 15, it has the same deficiency as claim 1.

iv. As per claim 6, lines 1-2, it is unclear whether "a main thread" is the same as "a main thread" referred to in claim 1(i.e. if it is the same it should be referred to as the main thread).

vii. As per claim 5, line 2, it is not clearly understood what is meant by "allocating in a bottom up order"? (i.e. from the leading thread of last tier in the thread chain).

viii. As per claim 12, they have the same deficiency as claim 5.

ix. As per claim 17, they have the same deficiency as claim 5.

x. As per claim 7, line 2, it is unclear how "determining whether there are resources remaining "will be done? (i.e. check the data structure of the child

threads). Line 4, it is unclear what are the criteria for "deleting at least one child of the current thread"? (i.e. insufficient resource for the current thread?).

xi. As per claim 14, it has the same deficiency as claim 7.

xii. As per claim 19, it has the same deficiency as claim 7.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1-6, 8-13 and 15-18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mulder ("inter: An inexpensive inter-procedural register allocator" Micro processing and microprogramming, Elsevier Science Publishers, Vol. 27, 1998, Pages 95-100), in view of Gouriou et al. (US 7,415,699 B2).

12. Mulder ("inter: An inexpensive inter-procedural register allocator" Micro processing and microprogramming, Elsevier Science Publishers, Vol. 27, 1998, Pages 95-100) was submitted by applicant in IDS filed on 01/24/2005.

13. As per claim, Mulder teaches the invention substantially as claimed including a method, comprising:

Generating, during a compilation of a code having , one or more threads executable in a

data processing system;

selecting a current thread having a most bottom order from the one and more threads (pg.95, section 1.3, lines 7-9; pg. 98, section 6, lines 3-5);

determining resources allocated to one or more child threads spawned from the current thread (pg. 98, section 6, lines 3-6; pg. 98, section 6.1, lines 2-4); and

allocating resources for the current thread in consideration of the resources allocated to the current thread's one or more child threads to avoid resource conflicts between the current thread and its one or more child threads (pg. 98, section 6.1, lines 1-2; pg. 98, section 6.1, lines 5-10).

14. Mulder doesn't explicitly teach having a main thread and each of the one or more threads including instructions copied from the main thread and that the method is done on threads.

15. However, Gouriou teaches that having a main thread and each of the one or more threads including instructions copied from the main thread (col. 10, lines 5-8).

16. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Mulder and Gouriou because Gouriou teaching of having a main thread and each of the one or more threads including instructions copied from the main thread is forking which is having instruction copied from main thread to child threads to act as helper threads to the main threads and since procedures are sequence of threads, it would be obvious to one of ordinary skill in the art at the time the invention was made to incorporate Mulder teaching of

inter procedural resource allocation in inter thread resource allocation because Mulder teaching would improve system performance, reducing system traffic and eliminate resource allocation conflicts.

17. As per claim 2, Mulder teaches that the resources include at least one of hardware registers and memory used by at least one of the one or more child threads (pg. 98, section 6, lines 3-6).

18. As per claim 3, Mulder teaches that wherein the resources allocated to the one or more child threads are recorded in a data structure accessible by the current thread (pg. 98, section 6.1, lines 5-10; pg. 99, section 6.3, subsection: separate compilation, lines 8-14)..

19. Mulder doesn't explicitly teach one or more child threads are recorded in a data structure. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to conclude from Mulder teaching of passing register usage information of child threads on interface files would improve system performance by eliminating resource allocation conflicts.

20. As per claim 4, Mulder teaches updating resource information in a data structure regarding the resources allocated to the current thread, the data structure being accessible by a parent thread of the current thread (pg. 98, section 6, lines 3-5; pg.98, section 6.1, lines 1-6; pg.

99, section 6.3, subsection: separate compilation, lines 9-14).

21. As per claim 5, Mulder teaches that repeating the selecting, determining, and allocating in a bottom-up order until each of the one or more threads has been processed (pg. 98, section 6, lines 3-5; pg. 98, section 6.1, lines 1-2).

22. As per claim 6, Mulder teaches allocate resources for a main thread that is a parent thread of the one or more threads after each of the one or more threads has been processed, the resources of the main thread are allocated in view of resources allocated to the one or more threads (pg. 98, section 6, lines 1-2; pg. 98, section 6.1, lines 5-10).

23. As per claims 8-13, they are the machine-readable storage medium claim of the method claims 1-6 respectively. Therefore, they are rejected under the same rational.

24. As per claim 15, Mulder teaches a data processing system, comprising:
a processor capable of performing multi-threading operations; a memory coupled to the processor (pg. 95, section 1.1, lines 1-4); and
a process executed by the processor from the memory to cause the processor to

generate, during a compilation of a code having, one or more threads executable in a data processing system,

select a current thread having a most bottom order from the one and more threads (pg. 95, section 1.3, lines 7-9; pg 98, section 6, lines 3-5);

determine resources allocated to one or more child threads spawned from the current thread (pg. 98, section 6, lines 3-6; pg. 98, section 6.1, lines 2-4), and

allocate resources for the current thread in consideration of the resources allocated to the current thread's one or more child threads to avoid resource conflicts between the current thread and its one or more child threads (pg. 98, section 6.1, lines 1-2; pg. 98, section 6.1, lines 5-10).

25. Mulder doesn't explicitly teach having a main thread and each of the one or more threads including instructions copied from the main thread and that the method is done on threads.

26. However, Gouriou teaches that having a main thread and each of the one or more threads including instructions copied from the main thread (col. 10, lines 5-8).

27. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Mulder and Gouriou because Gouriou teaching of having a main thread and each of the one or more threads including instructions copied from the main thread is forking which is having instruction copied from main thread to child threads to act as helper threads to the main threads and since procedures are sequence of threads, it would be obvious to one of ordinary skill in the art at the time the invention was made to incorporate Mulder teaching of inter procedural resource allocation in inter thread resource allocation because Mulder teaching would improve system performance, reducing system traffic and eliminate resource allocation conflicts.

28. As per claims 16-18, they are the data processing system claim of the method claims 4-6 respectively. Therefore, they are rejected under the same rational.

29. As per claim 20, it is the data processing system claim of the method claim 2. Therefore, it is rejected under the same rational.

30. Claims 7, 14 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mulder ("inter: An inexpensive inter-procedural register allocator" Micro processing and microprogramming, Elsevier Science Publishers, Vol. 27, 1998, Pages 95-100), in view of Gouriou et al. (US 7,415,699 B2) and further in view of Patterson (US 7,036,124 B1).

31. As per claim 7, the combined teaching doesn't explicitly teach determining whether there are resources remaining in the data processing system prior to the allocating the resources for the current thread; and deleting at least one child thread of the current thread; and allocating the resources for the current thread using the resources associated with the at least one deleted child thread.

32. However, Paterson teaches deleting at least one child thread of the current thread (abs., lines 8-10); and allocating the resources for the current thread using the resources associated with the at least one deleted child thread (abs., lines 8-12).

33. it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Mulder, Gouriou and Paterson teachings because Patterson's teaching of deleting at least one child thread of the current thread; and allocating the resources for the current thread using the resources associated with the at least one deleted child thread will improve system performance and resource allocation techniques since allocating the child's resource to the parent for accomplishing a higher priority task.

34. The combined teaching doesn't explicitly teach determining whether there are resources remaining in the data processing system prior to the allocating the resources for the current thread. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make use of Mulder, Gouriou and Paterson teaching of passing register information to the current thread to conclude that this information is used to determine what resources are used and what is remained available because determining available resources before allocation improve system efficiency and eliminate resource conflict.

35. As per claim 14, it is the machine-readable storage medium of the method claim 7. Therefore, it is rejected under the same rational.

36. As per claim 19, it is the data processing system of the method claim 7. Therefore, it is rejected under the same rational.

Response to Arguments

37. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

38. In the remarks applicant argues that:

(1) Muler fails to teach or suggest the limitation of determining shareable resource between a current thread based on instruction from a main thread for resource allocation.

(2) Paterson fails to teach determining shareable resources between a current thread and a child thread.

(3) Paterson fails to disclose that thread is deleted and instead it discloses that the thread is terminated.

39. Examiner respectfully disagree with the applicant :

i. As per point (1) and (2), it is noted that the features upon which applicant relies (i.e., resource include sharable resources between the current thread and the one or more child threads) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

ii. As per point (3), Applicant supports his argument that deleting may result in terminating and not the reverse. Termination in the context of the prior art is deleting

since the resource of the deleted thread is re-allocated to the parent process.

Conclusion

40. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

41. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

42. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CAROLINE ARCOS whose telephone number is (571)270-3151. The examiner can normally be reached on Monday-Thursday 7:00 AM to 5:30 PM.

43. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

44. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195

/Caroline Arcos/
Examiner, Art Unit 2195